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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

(1) Claim 1 has been amended as follows:

1. (Twice amended) A process for manufacturing an integrated circuit package comprising:

(a) forming a substrate having a first dielectric layer, a conductive layer having a first region insulated from a second region and located above the first dielectric layer, and a second dielectric layer above the conductive layer, the second dielectric layer having a cavity wherein the first and second regions are exposed within the cavity and the first region insulated from the second region by a third dielectric layer; and

(b) interconnecting a first lead of an integrated circuit to the exposed first region and interconnecting a second lead of the integrated circuit to the exposed second region.

(2) Claim 7 has been amended as follows:

7. (Twice amended) A method of manufacturing a substrate adapted to receive an integrated circuit chip comprising:

(a) forming a first dielectric layer on a substrate;

(b) forming a conductive layer having a first region insulated from a second region, above the first dielectric layer;

(c) forming a second dielectric layer above the conductive layer; and

(d) forming a cavity in the second dielectric layer to expose the first and second regions of the conductive layer and coupling a first lead of the integrated circuit chip to the exposed first region and coupling a second lead of the integrated circuit to the exposed second region, the first region insulated from the second region by a third dielectric layer.